

# DATA SHEET



## **PCA9553**

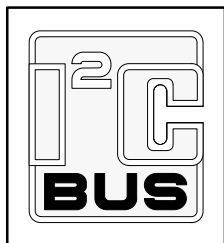
4-bit I<sup>2</sup>C LED driver with programmable  
blink rates

Product data  
Supersedes data of 2002 Dec 13

2003 May 02

# 4-bit I<sup>2</sup>C LED driver with programmable blink rates

## PCA9553



### FEATURES

- 4 LED drivers (on, off, flashing at a programmable rate)
- 2 selectable, fully programmable blink rates (frequency and duty cycle) between 0.15625 and 40 Hz (6.4 and 0.025 seconds)
- Input/outputs not used as LED drivers can be used as regular GPIOs
- Internal oscillator requires no external components
- I<sup>2</sup>C-businterface logic compatible with SMBus
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- 4 open drain outputs directly drive LEDs to 25 mA
- Controlled edge rates to minimize ground bounce
- No glitch on power-up
- Supports hot insertion
- Low stand-by current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8

### DESCRIPTION

The PCA9553 LED Blinker blinks LEDs in I<sup>2</sup>C and SMBus applications where it is necessary to limit bus traffic or free up the I<sup>2</sup>C Master's (MCU, MPU, DSP, chipset, etc.) timer. The uniqueness of this device is the internal oscillator with two programmable blink rates. To blink LEDs using normal I/O Expanders like the PCF8574 or PCA9554, the bus master must send repeated commands to turn the LED on and off. This greatly increases the amount of traffic on

the I<sup>2</sup>C-bus and uses up one of the master's timers. The PCA9553 LED Blinker instead requires only the initial set-up command to program BLINK RATE 1 and BLINK RATE 2 (i.e., the frequency and duty cycle). From then on, only one command from the bus master is required to turn each individual open drain output ON, OFF, or to cycle at BLINK RATE 1 or BLINK RATE 2. Maximum output sink current is 25 mA per bit and 100 mA per package.

Any bits not used for controlling the LEDs can be used for General Purpose Parallel Input/Output (GPIO) expansion.

Power On Reset (POR) initializes the registers to their default state, all zeroes, causing the bits to be set HIGH (LED off).

Due to pin limitations, the PCA9553 is not featured with hardware address pins. The PCA9553/01 and the PCA9553/02 have different fixed I<sup>2</sup>C-bus addresses allowing operation of both on the same bus.

### PIN CONFIGURATION

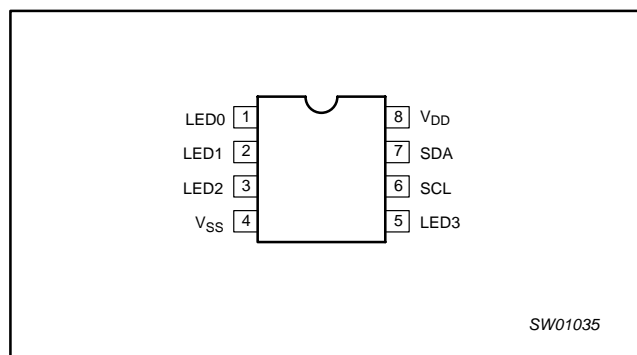


Figure 1. Pin configuration

### PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	LED0	LED driver 0
2	LED1	LED driver 1
3	LED2	LED driver 2
4	V <sub>SS</sub>	Supply ground
5	LED3	LED driver 3
6	SCL	Serial clock line
7	SDA	Serial data line
8	V <sub>DD</sub>	Supply voltage

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
8-Pin Plastic SO	-40 to +85 °C	PCA9553D/01	P9553/1	SOT96-1
8-Pin Plastic SO	-40 to +85 °C	PCA9553D/02	P9553/2	SOT96-1
8-Pin Plastic TSSOP	-40 to +85 °C	PCA9553DP/01	P53/1	SOT505-1
8-Pin Plastic TSSOP	-40 to +85 °C	PCA9553DP/02	P53/2	SOT505-1

Standard packing quantities and other packaging data is available at [www.philipslogic.com/packaging](http://www.philipslogic.com/packaging).

I<sup>2</sup>C is a trademark of Philips Semiconductors Corporation.

4-bit I<sup>2</sup>C LED driver with programmable blink rates

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## BLOCK DIAGRAM

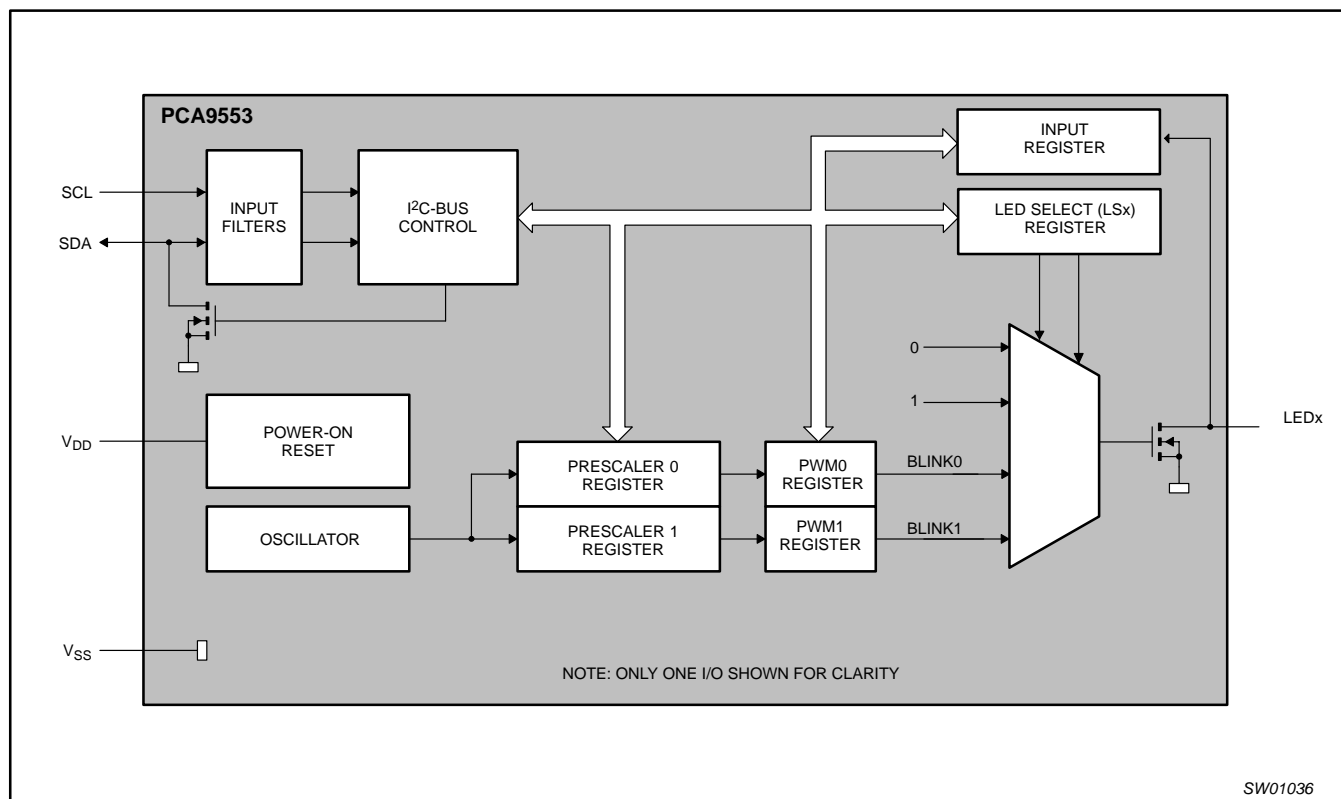


Figure 2. Block diagram

4-bit I<sup>2</sup>C LED driver with programmable blink rates

## PCA9553

## DEVICE ADDRESSING

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9553/01 is shown in Figure 3 and PCA9553/02 in Figure 4.

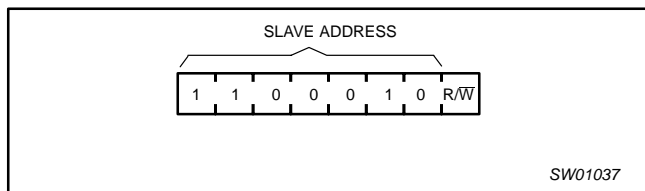


Figure 3. Slave address — PCA9553/01

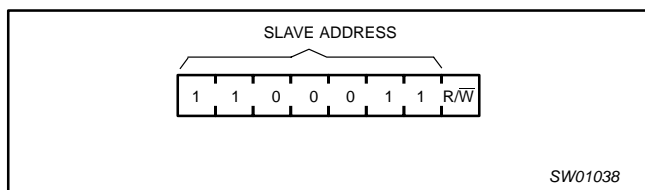


Figure 4. Slave address — PCA9553/02

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

## CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9553 which will be stored in the Control Register.

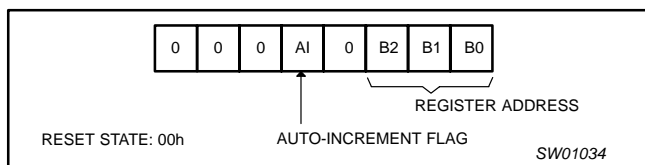


Figure 5. Control register

## CONTROL REGISTER DEFINITION

B2	B1	B0	REGISTER NAME	TYPE	REGISTER FUNCTION
0	0	0	INPUT	READ	INPUT REGISTER
0	0	1	PSC0	READ/ WRITE	FREQUENCY PRESCALER 0
0	1	0	PWM0	READ/ WRITE	PWM REGISTER 0
0	1	1	PSC1	READ/ WRITE	FREQUENCY PRESCALER 1
1	0	0	PWM1	READ/ WRITE	PWM REGISTER 1
1	0	1	LS0	READ/ WRITE	LED SELECTOR

## REGISTER DESCRIPTION

The lowest 3 bits are used as a pointer to determine which register will be accessed.

If the auto-increment flag is set, the three low order bits of the Control Register are automatically incremented after a read or write. This allows the user to program the registers sequentially. The

contents of these bits will rollover to '000' after the last register is accessed.

When auto-increment flag is set (AI = 1) and a read sequence is initiated, the sequence must start by reading a register different from '0' (B2 B1 B0 ≠ 0 0 0)

Only the 3 least significant bits are affected by the AI flag.

Unused bits must be programmed with zeroes.

## INPUT — INPUT REGISTER

bit	7	6	5	4	3	2	1	0
Default	X	X	X	X	X	X	X	X

The INPUT register reflects the state of the device pins. Writes to this register will be acknowledged but will have no effect.

## PSC0 — FREQUENCY PRESCALER 0

bit	7	6	5	4	3	2	1	0
default	1	1	1	1	1	1	1	1

PSC0 is used to program the period of the PWM output.

$$\text{The period of BLINK0} = \frac{(PSC0 + 1)}{44}$$

## PWM0 — PWM REGISTER 0

bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0

The PWM0 register determines the duty cycle of BLINK0. The outputs are LOW (LED off) when the count is less than the value in PWM0 and HIGH when it is greater. If PWM0 is programmed with 00h, then the PWM0 output is always LOW.

$$\text{The duty cycle of BLINK0 is: } \frac{256 - PWM0}{256}$$

## PSC1 — FREQUENCY PRESCALER 1

bit	7	6	5	4	3	2	1	0
default	1	1	1	1	1	1	1	1

PSC1 is used to program the period of PWM output.

$$\text{The period of BLINK1} = \frac{(PSC1 + 1)}{44}$$

## PWM1 — PWM REGISTER 1

bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0

The PWM1 register determines the duty cycle of BLINK1. The outputs are LOW (LED off) when the count is less than the value in PWM1 and HIGH when it is greater. If PWM1 is programmed with 00h, then the PWM1 output is always LOW.

$$\text{The duty cycle of BLINK1 is: } \frac{256 - PWM1}{256}$$

## LS0 — LED SELECTOR

	LED3		LED2		LED 1		LED 0	
bit	7	6	5	4	3	2	1	0
default	0	1	0	1	0	1	0	1

The LSx LED select registers determine the source of the LED data.

00 = Output is set LOW (LED on)

01 = Output is set Hi-Z (LED off - default)

10 = Output blinks at PWM0 rate

11 = Output blinks at PWM1 rate

4-bit I<sup>2</sup>C LED driver with programmable blink rates

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POWER-ON RESET

When power is applied to V<sub>DD</sub>, an internal Power-On Reset holds the PCA9553 in a reset state until V<sub>DD</sub> has reached V<sub>POR</sub>. At this point, the reset condition is released and the PCA9553 registers are initialized to their default states, with all outputs in the off state.

CHARACTERISTICS OF THE I<sup>2</sup>C-BUS

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 6).

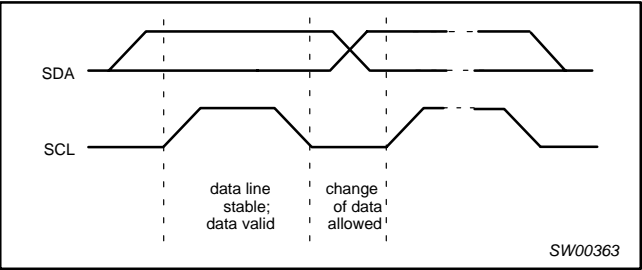


Figure 6. Bit transfer

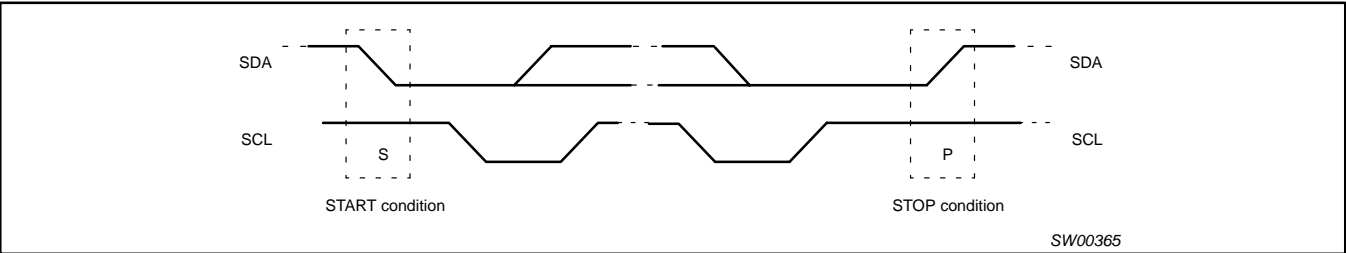


Figure 7. Definition of start and stop conditions

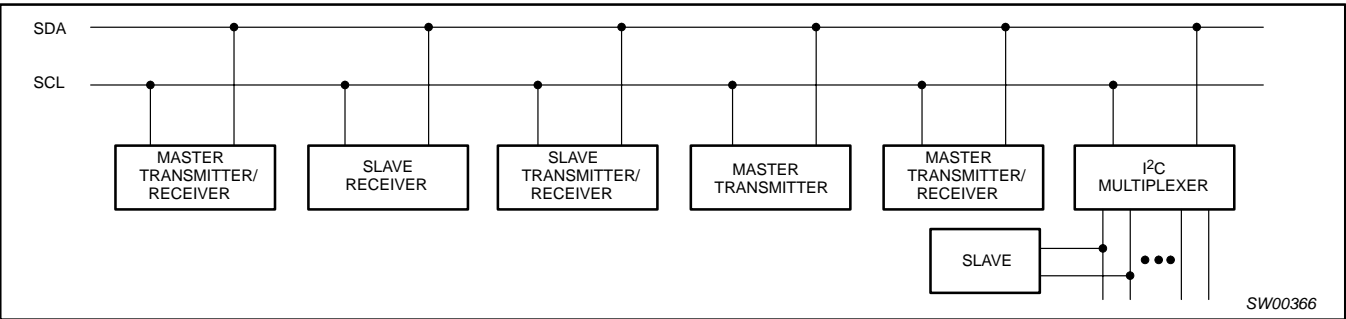


Figure 8. System configuration

4-bit I<sup>2</sup>C LED driver with programmable blink rates

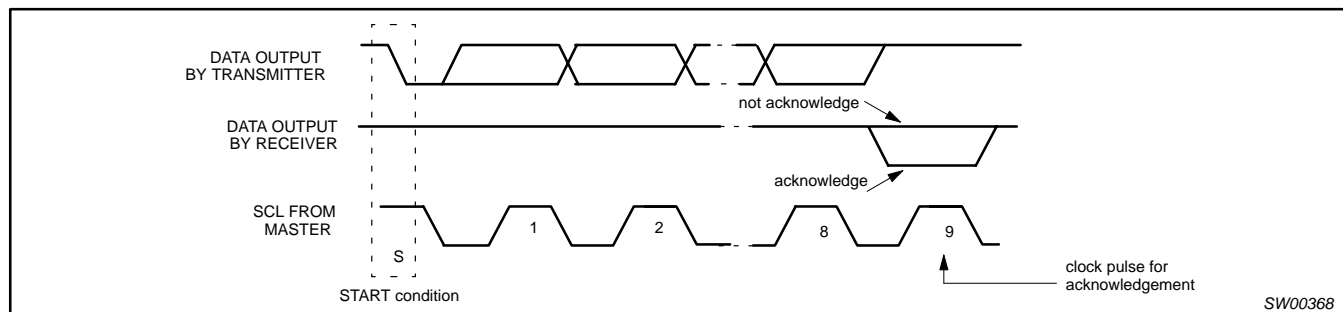
## PCA9553

**Acknowledge**

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.



**Figure 9. Acknowledgement on the I<sup>2</sup>C-bus**

4-bit I<sup>2</sup>C LED driver with programmable blink rates

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## Bus transactions

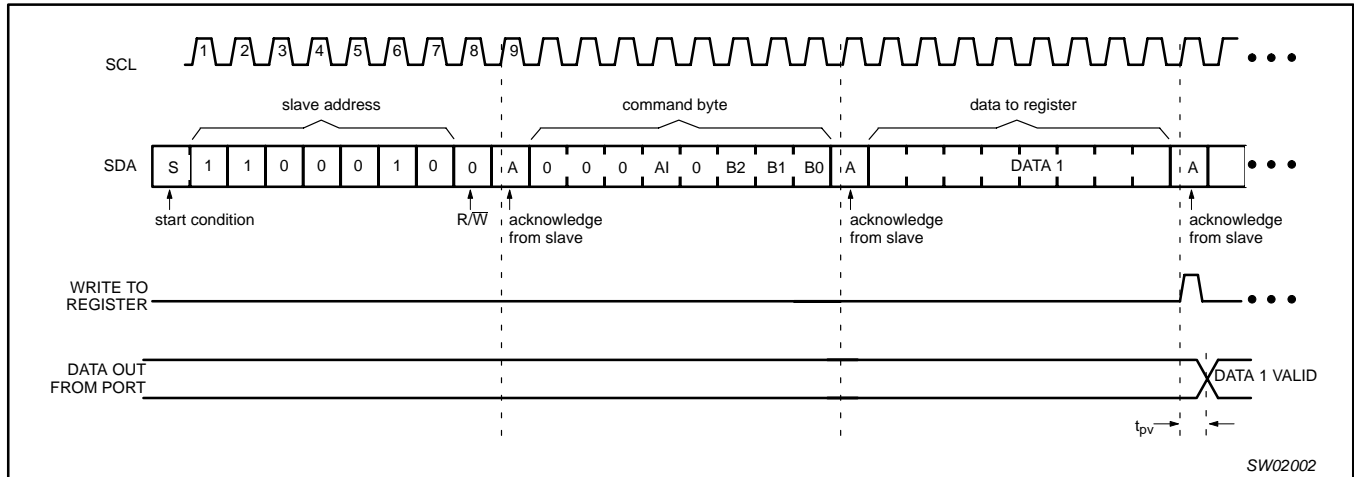


Figure 10. WRITE to register

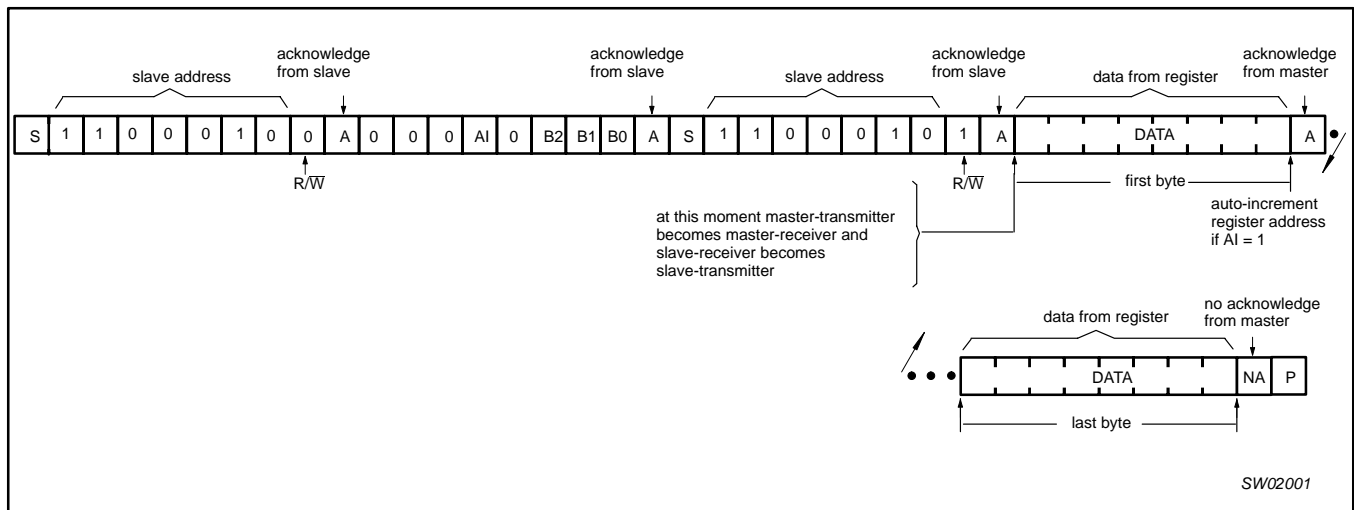
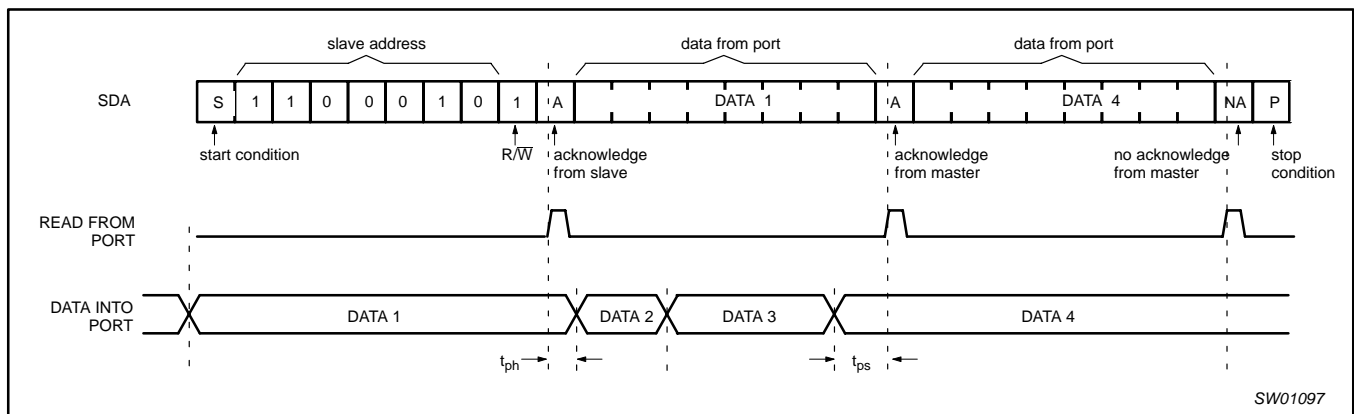


Figure 11. READ from register



## NOTES:

1. This figure assumes the command byte has previously been programmed with 00h.
2. PCA9553/01 shown.

Figure 12. READ input port register

# 4-bit I<sup>2</sup>C LED driver with programmable blink rates

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## APPLICATION DATA

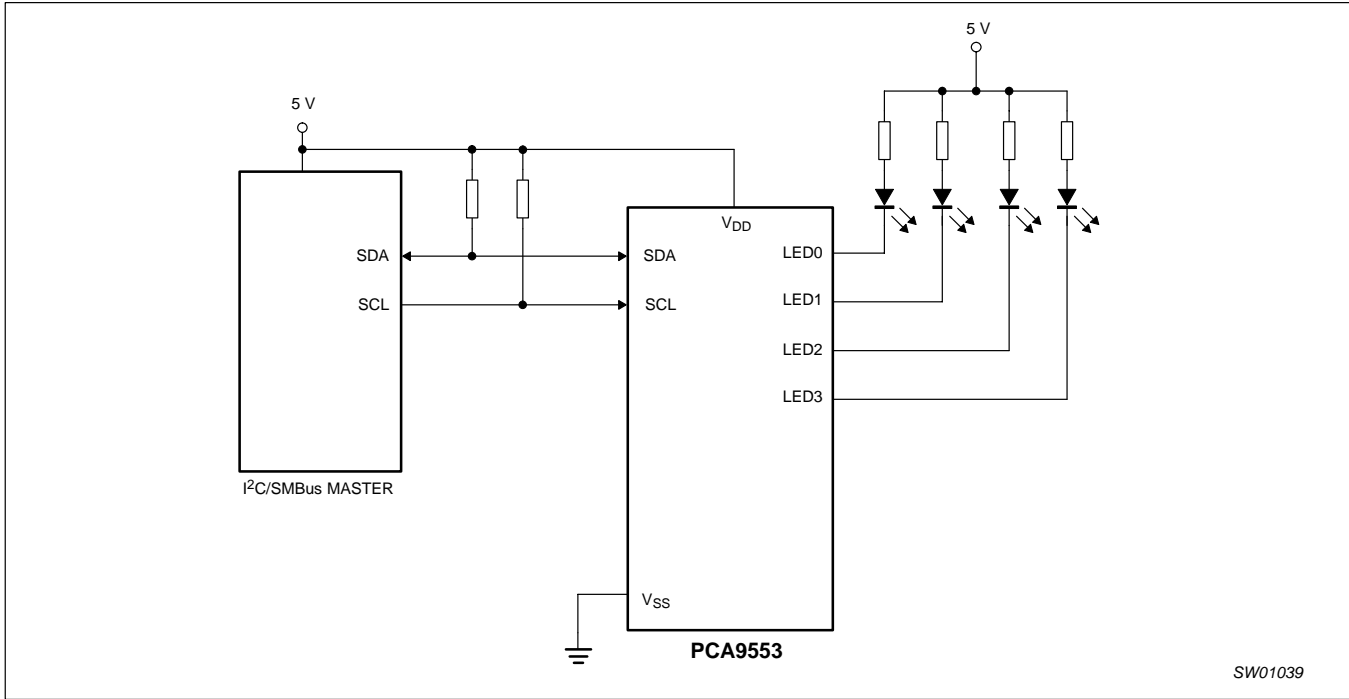


Figure 13. Typical application

### Minimizing $I_{DD}$ when the I/O is used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to  $V_{DD}$  through a resistor as shown in Figure 13. Since the LED acts as a diode, when the LED is off the I/O  $V_{IN}$  is about 1.2 V less than  $V_{DD}$ . The supply current,  $I_{DD}$ , increases as  $V_{IN}$  becomes lower than  $V_{DD}$  and is specified as  $\Delta I_{DD}$  in the DC characteristics table.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to  $V_{DD}$  when the LED is off. Figure 14 shows a high value resistor in parallel with the LED. Figure 15 shows  $V_{DD}$  less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O  $V_{IN}$  at or above  $V_{DD}$  and prevents additional supply current consumption when the LED is off.

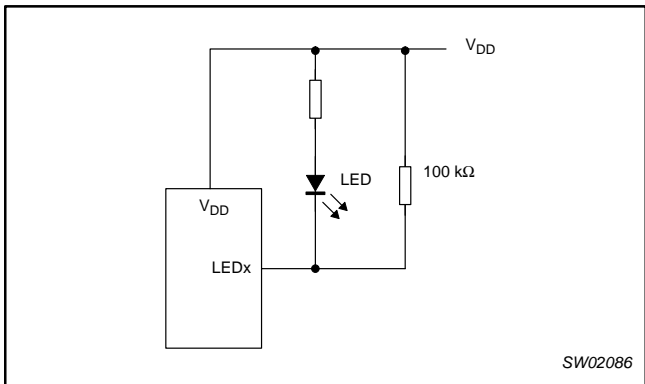


Figure 14. High value resistor in parallel with the LED

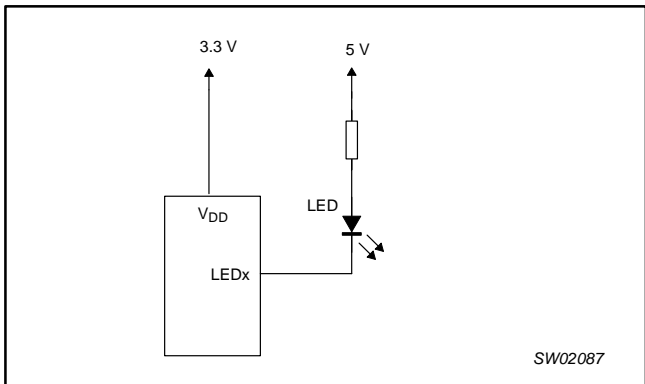


Figure 15. Device supplied by a lower voltage



4-bit I<sup>2</sup>C LED driver with programmable blink rates

## PCA9553

**Programming example**

The following example will show how to set LED0 and LED1 off. It will then set LED2 to blink at 1 Hz, 50% duty cycle. LED3 will be set to blink at 4 Hz, 25% duty cycle. PCA9553/01 is used in this example.

**Table 1.**

	I <sup>2</sup> C-bus
Start	S
PCA9553 address	C4h
PSC0 subaddress + auto-increment	11h
Set prescaler PSC0 to achieve a period of 1 second: $\text{Blink period} = 1 = \frac{\text{PSC0} + 1}{44}$ PSC0 = 37	25h
Set PWM0 duty cycle to 50%: $\frac{256 - \text{PWM0}}{256} = 0.5$ PWM0 = 128	80h
Set prescaler PWM1 to achieve a period of 0.25 seconds: $\text{Blink period} = 0.25 = \frac{\text{PSC1} + 1}{44}$ PSC1 = 9	09h
Set PWM1 output duty cycle to 25%: $\frac{256 - \text{PWM1}}{256} = 0.25$ PWM1 = 192	C0h
Set LED0 on, LED1 off, LED2 set to blink at PSC0, PWM0, LED3 set to blink at PCS1, PWM1	E4h
Stop	P

4-bit I<sup>2</sup>C LED driver with programmable blink rates

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## ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage		-0.5	6.0	V
V <sub>I/O</sub>	DC voltage on an I/O		V <sub>SS</sub> - 0.5	5.5	V
I <sub>I/O</sub>	DC output current on an I/O		—	±25	mA
I <sub>SS</sub>	Supply current		—	100	mA
P <sub>tot</sub>	Total power dissipation		—	400	mW
T <sub>stg</sub>	Storage temperature range		-65	+150	°C
T <sub>amb</sub>	Operating ambient temperature		-40	+85	°C

## HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "Handling MOS devices".

## DC CHARACTERISTICS

V<sub>DD</sub> = 2.3 to 5.5 V; V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 to +85 °C; unless otherwise specified. TYP at 3.3 V and 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
<b>Supplies</b>						
V <sub>DD</sub>	Supply voltage		2.3	—	5.5	V
I <sub>DD</sub>	Supply current	Operating mode; V <sub>DD</sub> = 5.5 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 100 kHz	—	350	500	μA
I <sub>stb</sub>	Standby current	Standby mode; V <sub>DD</sub> = 5.5 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 100 kHz	—	1.9	3.0	μA
ΔI <sub>DD</sub>	Additional standby current	Standby mode; V <sub>DD</sub> = 5.5 V; Every LED I/O at V <sub>IN</sub> = 4.3 V; f <sub>SCL</sub> = 0 kHz	—	—	325	μA
V <sub>POR</sub>	Power-on reset voltage	No load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	—	1.7	2.2	V
<b>Input SCL; input/output SDA</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	—	0.3 V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7 V <sub>DD</sub>	—	5.5	V
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V	3	6.5	—	mA
I <sub>L</sub>	Leakage current	V <sub>I</sub> = V <sub>DD</sub> = V <sub>SS</sub>	-1	—	+1	μA
C <sub>I</sub>	Input capacitance	V <sub>I</sub> = V <sub>SS</sub>	—	3.7	5	pF
<b>I/Os</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	—	0.8	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	—	5.5	V
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V; V <sub>DD</sub> = 2.3 V; Note 1	9	—	—	mA
		V <sub>OL</sub> = 0.4 V; V <sub>DD</sub> = 3.0 V; Note 1	12	—	—	mA
		V <sub>OL</sub> = 0.4 V; V <sub>DD</sub> = 4.5 V; Note 1	15	—	—	mA
		V <sub>OL</sub> = 0.7 V; V <sub>DD</sub> = 2.3 V; Note 1	15	—	—	mA
		V <sub>OL</sub> = 0.7 V; V <sub>DD</sub> = 3.0 V; Note 1	20	—	—	mA
		V <sub>OL</sub> = 0.7 V; V <sub>DD</sub> = 4.5 V; Note 1	25	—	—	mA
I <sub>L</sub>	Input leakage current	V <sub>DD</sub> = 3.6 V; V <sub>I</sub> = 0 or V <sub>DD</sub>	-1	—	1	μA
C <sub>IO</sub>	Input/output capacitance		—	2.1	5	pF

## NOTES:

- Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

4-bit I<sup>2</sup>C LED driver with programmable blink rates

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## AC SPECIFICATIONS

SYMBOL	PARAMETER	STANDARD MODE I <sup>2</sup> C BUS		FAST MODE I <sup>2</sup> C BUS		UNITS
		MIN	MAX	MIN	MAX	
$f_{SCL}$	Operating frequency	0	100	0	400	kHz
$t_{BUF}$	Bus free time between STOP and START conditions	4.7	—	1.3	—	$\mu$ s
$t_{HD;STA}$	Hold time after (repeated) START condition	4.0	—	0.6	—	$\mu$ s
$t_{SU;STA}$	Repeated START condition set-up time	4.7	—	0.6	—	$\mu$ s
$t_{SU;STO}$	Set-up time for STOP condition	4.0	—	0.6	—	$\mu$ s
$t_{HD;DAT}$	Data in hold time	0	—	0	—	ns
$t_{VD;ACK}$	Valid time for ACK condition <sup>2</sup>	—	600	—	600	ns
$t_{VD;DAT (L)}$	Data out valid time <sup>3</sup>	—	600	—	600	ns
$t_{VD;DAT (H)}$	Data out valid time <sup>3</sup>	—	1500	—	600	ns
$t_{SU;DAT}$	Data set-up time	250	—	100	—	ns
$t_{LOW}$	Clock LOW period	4.7	—	1.3	—	$\mu$ s
$t_{HIGH}$	Clock HIGH period	4.0	—	0.6	—	$\mu$ s
$t_F$	Clock/Data fall time	—	300	$20 + 0.1 C_b^1$	300	ns
$t_R$	Clock/Data rise time	—	1000	$20 + 0.1 C_b^1$	300	ns
$t_{SP}$	Pulse width of spikes that must be suppressed by the input filters	—	50	—	50	ns
<b>Port Timing</b>						
$t_{PV}$	Output data valid	—	200	—	200	ns
$t_{PS}$	Input data set-up time	100	—	100	—	ns
$t_{PH}$	Input data hold time	1	—	1	—	$\mu$ s

## NOTES:

- $C_b$  = total capacitance of one bus line in pF.
- $t_{VD;ACK}$  = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
- $t_{VD;DAT}$  = minimum time for SDA data out to be valid following SCL LOW.

4-bit I<sup>2</sup>C LED driver with programmable blink rates

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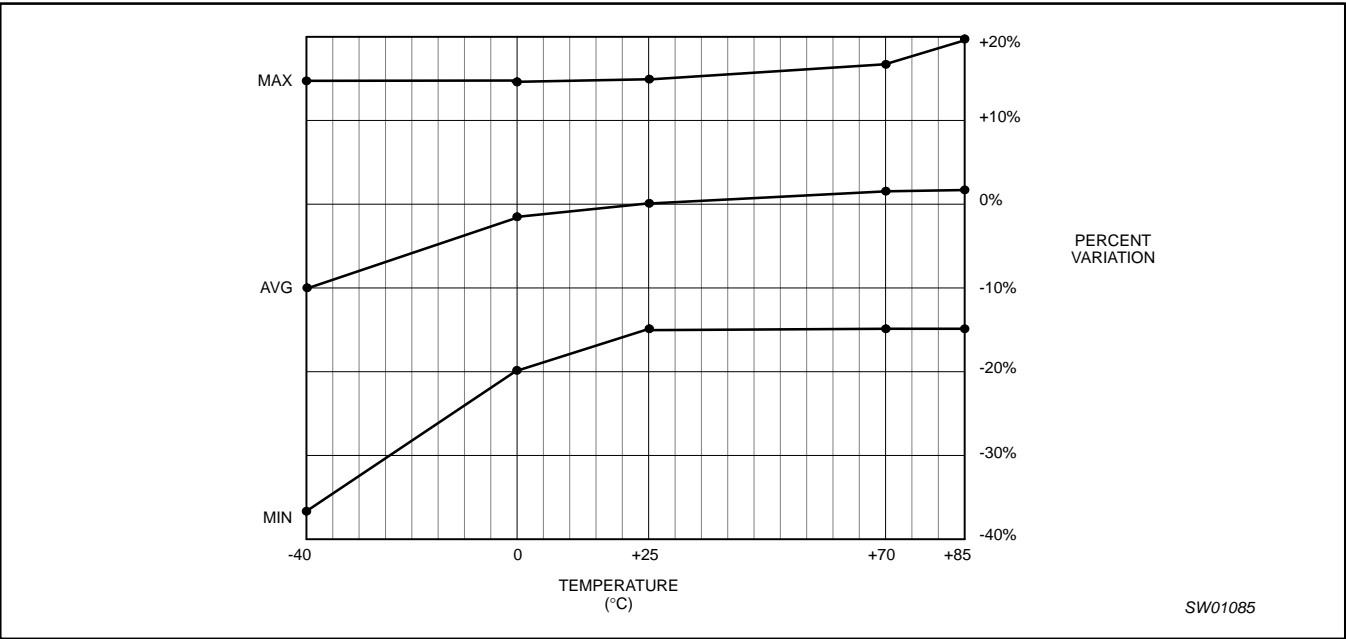


Figure 16. Typical frequency variation over process at  $V_{DD} = 2.3\text{ V to } 3.0\text{ V}$

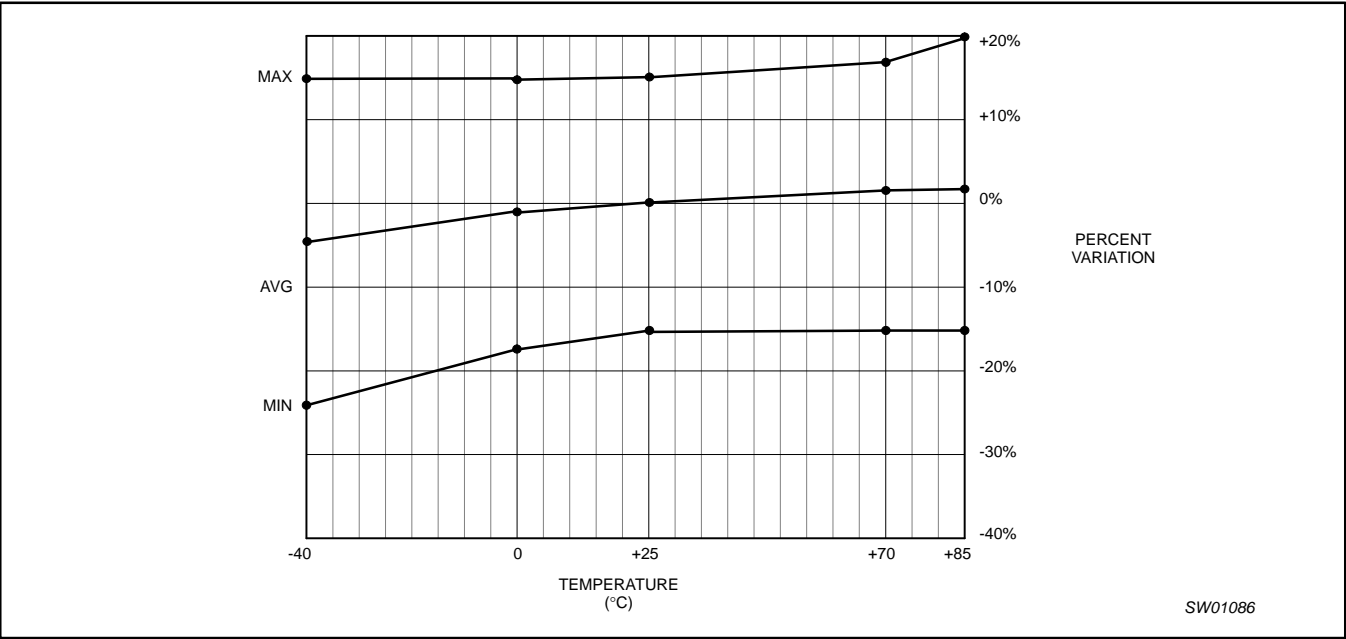


Figure 17. Typical frequency variation over process at  $V_{DD} = 3.0\text{ V to } 5.5\text{ V}$

4-bit I<sup>2</sup>C LED driver with programmable blink rates

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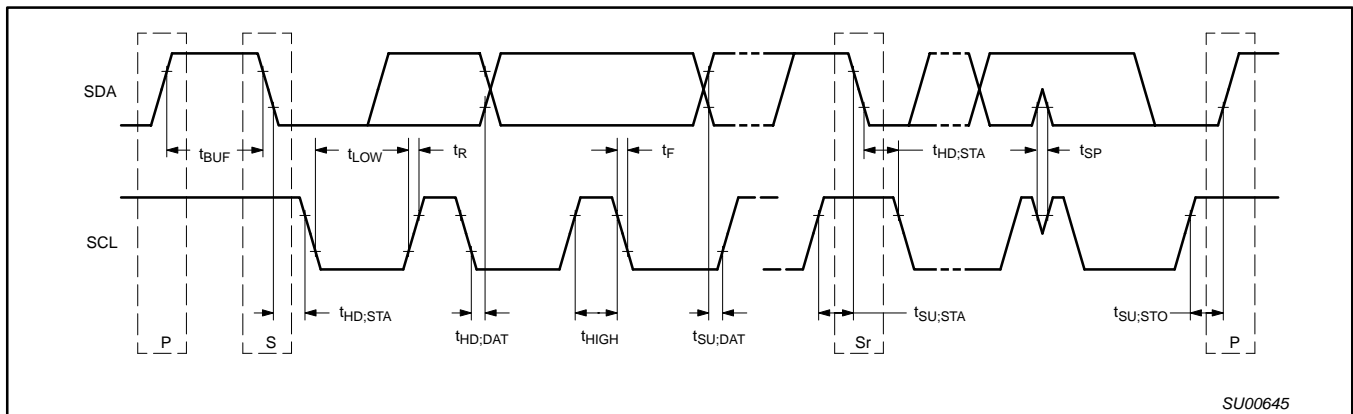


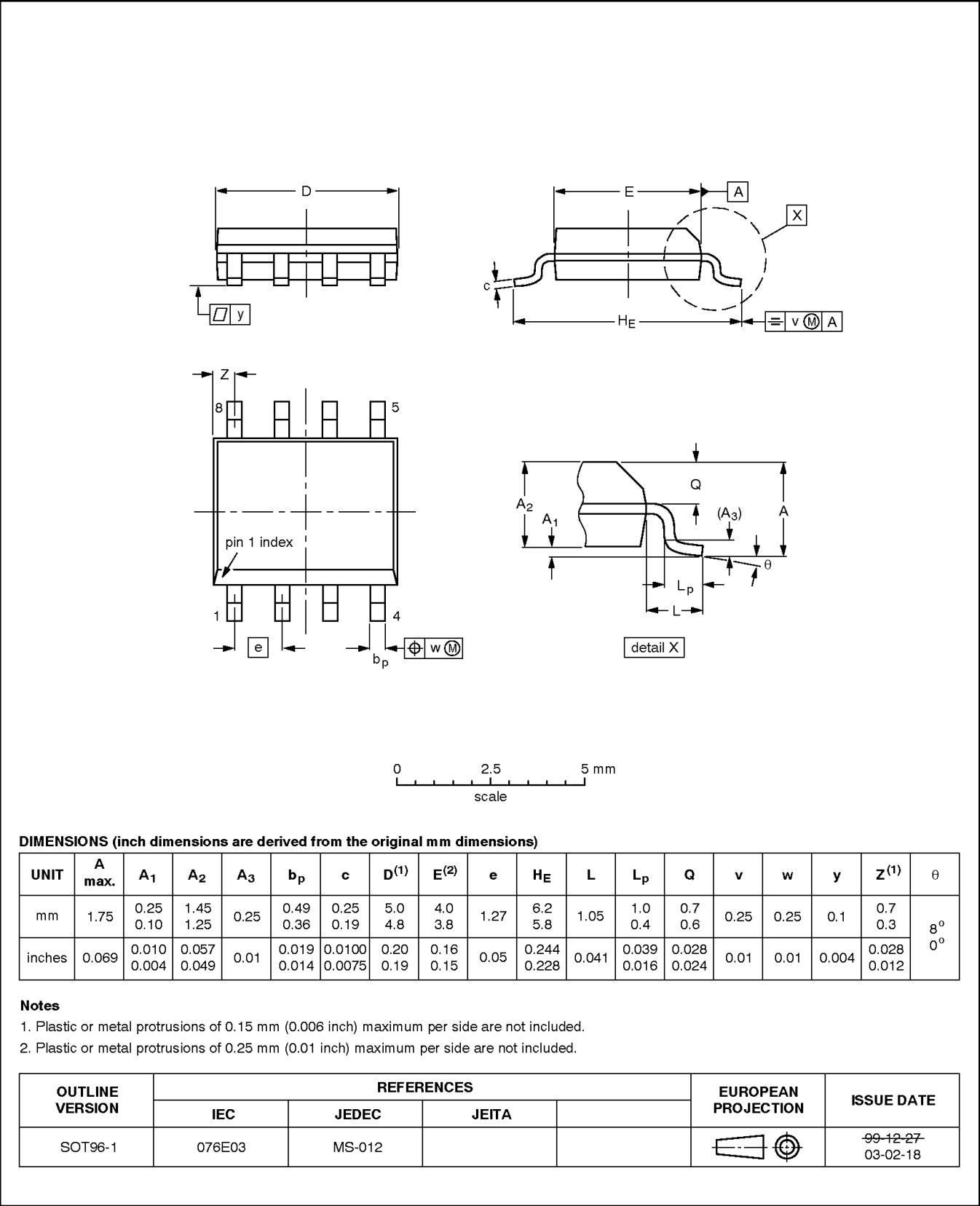
Figure 18. Definition of timing

4-bit I<sup>2</sup>C LED driver with programmable blink rates

PCA9553

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

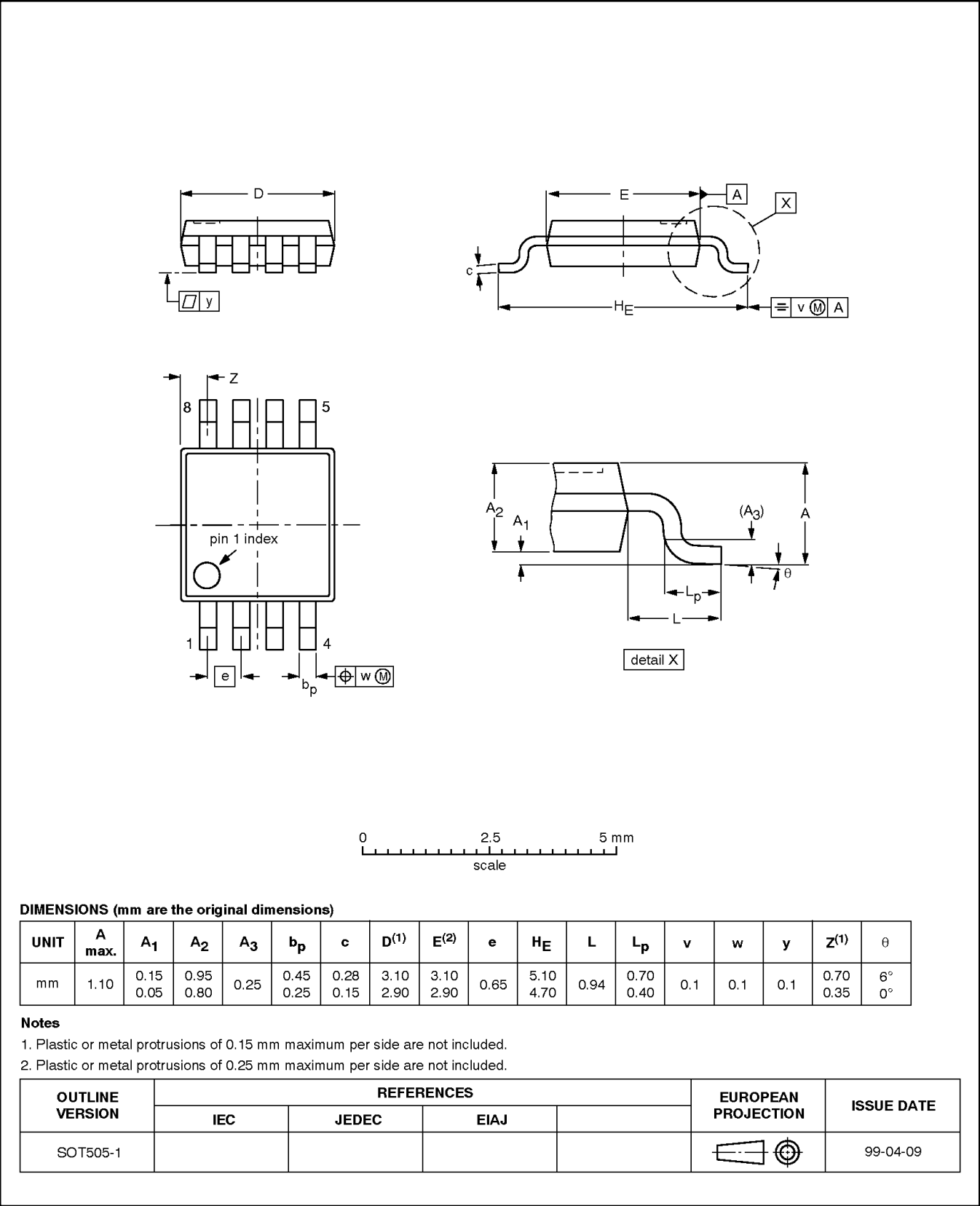


4-bit I<sup>2</sup>C LED driver with programmable blink rates

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TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1



4-bit I<sup>2</sup>C LED driver with programmable blink rates

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## REVISION HISTORY

Rev	Date	Description
_2	20030502	<b>Product data (9397 750 11464); ECN 853-2397 29856 Dated 24 April2003. Supersedes data of 2002 Dec 13 (9397 750 10859).</b> Modifications: <ul style="list-style-type: none"><li>• Correction to voltage in typical application drawing</li><li>• Update maximum current per bit and per device</li><li>• Adjust maximum and minimum curves to <math>\pm 15\%</math> on frequency variation graphs.</li></ul>
_1	20021213	Product data (9397 750 10859); ECN 853-2397 29264 of 09 December 2002.



4-bit I<sup>2</sup>C LED driver with programmable blink rates

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Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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